PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI

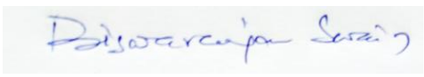
DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING

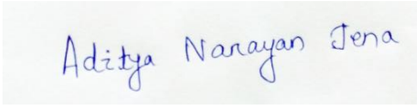
LESSON PLAN

BRANCH : **COMP. SC. & ENGINEERING**	**SEMESTER :** **3RD**	**NAME OF THE TEACHING FACULTY :** **MR. ADITYA NARAYAN JENA**
SUBJECT : **DIGITAL ELECTRONICS**	**NO. OF DAYS PER WEEK CLASS ALLOTTED : 05**	**SEMESTER FROM DATE: 01.07.2024 TO 08.11.2024**
WEEK	**CLASSDAY**	**THEORY TOPICS**
1ST	1st	**1.BASICS OF DIGITAL ELECTRONICS** NUMBER SYSTEM-BINARY, OCTAL, DECIMAL, HEXADECIMAL NUMBER SYSTEM
	2nd	CONVERSION OF BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM INTO DECIMAL NUMBER SYSTEM
	3rd	CONVERSION OF DECIMAL NUMBER SYSTEM INTO BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM
	4th	CONVERSION OF BINARY TO OCTAL, OCTAL TO BINARY, BINARY TO HEXADECIMAL,HEXADECIMAL NUMBER SYSTEM INTO BINARY NUMBER SYSTEM OCTAL TO HEXADECIMAL, HEXADECIMAL TO OCTAL NUMBER SYSTE
	5th	BINARY ARITHMATIC (ADDITION,SUBTRACTION,MULTIPLICATION,DIVISION)
2ND	1st	1'S COMPLEMENT,2'S COMPLEMENT AND SUBTRACTION OF BINARY NUMBER USING COMPLEMENT METHOD
	2nd	BINARY CODES(BCD,XS-3,GRAY CODE)
	3rd	LOGIC GATES(AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR)- SYMBOL,EXPRESSION, TRUTH TABLE AND TIMING DIAGRAM
	4th	UNIVERSAL GATES AND ITS REALIZATION (USING NAND GATES)
	5th	UNIVERSAL GATES AND ITS REALIZATION (USING NOR GATES).
3RD	1st	BOOLEAN ALGEBRA, BOOLEAN EXPRESSIONS, DEMORGAN'S THEOREM
	2nd	SOP,STANDARD SOP,MIN TERM
	3rd	POS,STANDARD POS,MAX TERM
	4th	2-VARIABLE,3-VARIABLE,4-VARIABLE K-MAP
	5th	SIMPLIFICATION OF SOP AND POS EXPRESSION USING K-MAP
4TH	1st	DON'T CARE CONDITIONS
	2nd	**2.COMBINATIONAL LOGIC CIRCUITS** CONCEPT OF CLC, HALF ADDER WORKING AND LOGIC DIAGRAM
	3rd	FULL ADDER WORKING,TRUTH TABLE,LOGIC DIAGRAM
	4th	HALF SUBTRACTOR,FULL SUBTRACTOR WORKING,TRUTH TABLE,LOGIC DIAGRAM

	5th	SERIAL AND PARALLEL BINARY 4-BIT ADDER WORKING
5TH	1st	REVISION
	2nd	DECODER,ENCODER
	3rd	4:1 MUX,1:4 DMUX WORKING,LOGIC DIAGRAM
	4th	2-BIT COMPARATOR,3-BIT COMPARATOR WORKING
	5th	SEVEN SEGMENT DECODER(CONCEPT,LOGIC CIRCUIT,TRUTH TABLE,APPLICATION)
6TH	1st	**3.SEQUENTIAL LOGIC CIRCUITS** SLC,TYPES OF SLC,DIFFERENCE BETWEEN CLC AND SLC,CONCEPT OF CLOCK AND TRIGGERING
	2nd	NOR BASED SR-FF AND NAND-BASED SR-FF WORKING
	3rd	CLOCKED SR FLIP-FLOP,D-FF WORKING
	4th	CLOCKED JK FLIP-FLOP WORKING,CLOCKED T-FF
	5th	RACE AROUND CONDITION,MASTER-SLAVE JK-FF WORKING,APPLICATION OF FLIP-FLOPS
7TH	1st	**4.REGISTERS, MEMORIES & PLD** SHIFT REGISTERS-SERIAL-IN SERIAL-OUT(SIPO) WORKING
	2nd	SERIAL-IN PARALLEL-OUT(SIPO)
	3rd	REVISION
	4th	PARALLEL-IN SERIAL-OUT (PIPO) WORKING
	5th	PARALLEL-IN PARALLEL-OUT (PIPO) WORKING
8TH	1st	UNIVERSAL SHIFT REGISTER AND ITS APPLICATION.
	2nd	DEFINE COUNTER, TYPES OF COUNTER AND ITS APPLICATIONS.
	3rd	4-BIT RIPPLE COUNTER WORKING,TIMING DIAGRAM
	4th	BINARY COUNTER WORKING
	5th	DECADE COUNTER WORKING
9TH	1st	REVISION
	2nd	SYNCHRONOUS COUNTER WORKING
	3rd	RING COUNTER WORKING
	4th	CONCEPT OF MEMORIES,TYPES
	5th	RAM,STATIC RAM, DYNAMIC RAM
10TH	1st	ROM,ITS TYPES
	2nd	BASIC CONCEPT OF PLD, APPLICATION PLD

	3rd	**5.A/D AND D/A CONVERTERS** NECESSITY OF A/D AND D/A CONVERTER
	4th	D/A CONVERSION USING WEIGHTED RESISTORS METHOD
	5th	D/A CONVERSION USING R-2R LADDER (WEIGHTED RESISTORS) NETWORK
11TH	1st	A/D CONVERSION USING COUNTER METHOD
	2nd	A/D CONVERSION USING SUCCESSIVE APPROXIMATE METHOD
	3rd	VARIOUS LOGIC FAMILIES & TYPES ACCORDING TO THE IC FABRICATION PROCESS
	4th	CHARACTERISTICS OF DIGITAL ICS-PROPAGATION DELAY, FAN- OUT, FAN-IN
	5th	POWER DISSIPATION, NOISE MARGIN, POWER SUPPLY REQUIREMENT, AND SPEED WITH REFERENCE TO LOGIC FAMILIES
12TH	1st	FEATURES, CIRCUIT OPERATION;APPLICATIONS OF TTL (NAND)
	2nd	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NAND)
	3rd	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NOR)
	4th	REVISION
	5th	REVISION





SIGNATURE OF H.O.D

SIGNATURE OF LECTURER