

<div>PNS SCHOOL OF ENGG. & TECH., MARSHAGHAI</div> <div>DEPARTMENT OF ELECTRONICS & TELECOMMUNICATION ENGINEERING</div> <div>LESSON PLAN</div>		
<div>BRANCH :</div> <div>ETC ENGG.</div>	<div>SEMESTER :</div> <div>3RD</div>	<div>NAME OF THE TEACHING FACULTY :</div> <div>MR. ADITYA NARAYAN JENA</div>
<div>SUBJECT :</div> <div>DIGITAL ELECTRONICS</div>	<div>NO. OF DAYS PER WEEK CLASS ALLOTTED :</div> <div>05</div>	<div>SEMESTER FROM DATE: 01.07.2024 TO 08.11.2024</div>
WEEK	CLASSDAY	THEORY TOPICS
1 ST	1 st	<div>1.BASICS OF DIGITAL ELECTRONICS</div> <div>NUMBER SYSTEM-BINARY, OCTAL, DECIMAL, HEXADECIMAL NUMBER SYSTEM</div>
	2 nd	CONVERSION OF BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM INTO DECIMAL NUMBER SYSTEM
	3 rd	CONVERSION OF DECIMAL NUMBER SYSTEM INTO BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM
	4 th	CONVERSION OF BINARY TO OCTAL, OCTAL TO BINARY, BINARY TO HEXADECIMAL,HEXADECIMAL NUMBER SYSTEM INTO BINARY NUMBER SYSTEM OCTAL TO HEXADECIMAL, HEXADECIMAL TO OCTAL NUMBER SYSTEM
	5 th	BINARY ARITHMATIC (ADDITION,SUBTRACTION,MULTIPLICATION,DIVISION)
2 ND	1 st	1'S COMPLEMENT,2'S COMPLEMENT AND SUBTRACTION OF BINARY NUMBER USING COMPLEMENT METHOD
	2 nd	BINARY CODES(BCD,XS-3,GRAY CODE)
	3 rd	LOGIC GATES(AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR)- SYMBOL,EXPRESSION, TRUTH TABLE AND TIMING DIAGRAM.
	4 th	UNIVERSAL GATES AND ITS REALIZATION (USING NAND GATES)
	5 th	UNIVERSAL GATES AND ITS REALIZATION (USING NOR GATES).
3 RD	1 st	BOOLEAN ALGEBRA, BOOLEAN EXPRESSIONS, DEMORGAN’S THEOREM
	2 nd	SOP,STANDARD SOP,MIN TERM
	3 rd	POS,STANDARD POS,MAX TERM
	4 th	2-VARIABLE,3-VARIABLE,4-VARIABLE K-MAP
	5 th	SIMPLIFICATION OF SOP AND POS EXPRESSION USING K-MAP
4 TH	1 st	DON’T CARE CONDITIONS.
	2 nd	<div>2.COMBINATIONAL LOGIC CIRCUITS</div> <div>CONCEPT OF CLC, HALF ADDER WORKING AND LOGIC DIAGRAM</div>
	3 rd	FULL ADDER WORKING,TRUTH TABLE,LOGIC DIAGRAM
	4 th	HALF SUBTRACTOR,FULL SUBTRACTOR WORKING,TRUTH TABLE,LOGIC DIAGRAM
	5 th	SERIAL AND PARALLEL BINARY 4-BIT ADDER WORKING

5 TH	1 st	REVISION
	2 nd	DECODER,ENCODER
	3 rd	4:1 MUX,1:4 DMUX WORKING,LOGIC DIAGRAM
	4 th	2-BIT COMPARATOR,3-BIT COMPARATOR WORKING
	5 th	SEVEN SEGMENT DECODER(CONCEPT,LOGIC CIRCUIT,TRUTH TABLE,APPLICATION)
6 TH	1 st	3.SEQUENTIAL LOGIC CIRCUITS SLC,TYPES OF SLC,DIFFERENCE BETWEEN CLC AND SLC,CONCEPT OF CLOCK AND TRIGGERING
	2 nd	NOR BASED SR-FF AND NAND-BASED SR-FF WORKING
	3 rd	CLOCKED SR FLIP-FLOP,D-FF WORKING
	4 th	CLOCKED JK FLIP-FLOP WORKING,CLOCKED T-FF
	5 th	RACE AROUND CONDITION,MASTER-SLAVE JK-FF WORKING,APPLICATION OF FLIP-FLOPS
7 TH	1 st	4.REGISTERS, MEMORIES & PLD SHIFT REGISTERS-SERIAL-IN SERIAL-OUT(SIPO) WORKING
	2 nd	SERIAL-IN PARALLEL-OUT(SIPO)
	3 rd	REVISION
	4 th	PARALLEL-IN SERIAL-OUT (PIPO) WORKING
	5 th	PARALLEL-IN PARALLEL-OUT (PIPO) WORKING
8 TH	1 st	UNIVERSAL SHIFT REGISTER AND ITS APPLICATION
	2 nd	DEFINE COUNTER, TYPES OF COUNTER AND ITS APPLICATIONS.
	3 rd	4-BIT RIPPLE COUNTER WORKING,TIMING DIAGRAM
	4 th	BINARY COUNTER WORKING
	5 th	DECADE COUNTER WORKING
9 TH	1 st	REVISION
	2 nd	SYNCHRONOUS COUNTER WORKING
	3 rd	RING COUNTER WORKING
	4 th	CONCEPT OF MEMORIES,TYPES
	5 th	RAM,STATIC RAM, DYNAMIC RAM
10 TH	1 st	ROM,ITS TYPES
	2 nd	BASIC CONCEPT OF PLD, APPLICATION PLD
	3 rd	5.A/D AND D/A CONVERTERS NECESSITY OF A/D AND D/A CONVERTER

	4 th	D/A CONVERSION USING WEIGHTED RESISTORS METHOD
	5 th	D/A CONVERSION USING R-2R LADDER (WEIGHTED RESISTORS) NETWORK
11 TH	1 st	A/D CONVERSION USING COUNTER METHOD
	2 nd	A/D CONVERSION USING SUCCESSIVE APPROXIMATE METHOD
	3 rd	VARIOUS LOGIC FAMILIES & TYPES ACCORDING TO THE IC FABRICATION PROCESS
	4 th	CHARACTERISTICS OF DIGITAL ICS-PROPAGATION DELAY, FAN- OUT, FAN-IN
	5 th	POWER DISSIPATION, NOISE MARGIN, POWER SUPPLY REQUIREMENT, AND SPEED WITH REFERENCE TO LOGIC FAMILIES
12 TH	1 st	FEATURES, CIRCUIT OPERATION;APPLICATIONS OF TTL (NAND)
	2 nd	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NAND)
	3 rd	FEATURES, CIRCUIT OPERATION; APPLICATIONS OF CMOS (NOR)
	4 th	REVISION
	5 th	REVISION

Amarendra Saha

SIGNATURE OF H.O.D

Aditya Narayan Jena

SIGNATURE OF LECTURER