

<b>PNS School of Engg. &amp; Tech, Marshaghai, Kendrapara</b> <b>LESSON PLAN</b> <b><u>Session (2024-2025)</u></b>		
<b>Discipline:</b> Computer Science & Engineering	<b>Semester-3rd</b>	<b>Name of the faculty:</b> Jayashree Bishoi
<b>Subject:</b> COMPUTER SYSTEM ARCHITECTURE(Th-1)	<b>No. of Days/week: 04</b>	<b>Start Date: 01/07/2024</b>
		<b>End Date: 08/11/2024</b>
<b>Week</b>	<b>Class Day</b>	<b>Theory Topics</b>
1 <sup>st</sup>	1 <sup>st</sup>	<b>1.Basic structure of computer hardware</b>
	2 <sup>nd</sup>	Basic Structure of computer hardware Introduction
	3 <sup>rd</sup>	Functional Units
	4 <sup>th</sup>	Computer components
2 <sup>nd</sup>	1 <sup>st</sup>	Memory addressing & Operations
	2 <sup>nd</sup>	Doubt clearing class & Question Answer Discussion
	3 <sup>rd</sup>	<b>2.Instructions &amp; instruction Sequencing</b>
	4 <sup>th</sup>	Fundamentals to instructions
3 <sup>rd</sup>	1 <sup>st</sup>	Operands
	2 <sup>nd</sup>	OpCodes
	3 <sup>rd</sup>	Instruction formats
	4 <sup>th</sup>	Addressing Modes
4 <sup>th</sup>	1 <sup>st</sup>	<b>3.Processor System</b>
	2 <sup>nd</sup>	Register Files
	3 <sup>rd</sup>	Complete instruction execution
	4 <sup>th</sup>	Fetch,Decode,Execution
5 <sup>th</sup>	1 <sup>st</sup>	Hardware controlled Unit
	2 <sup>nd</sup>	Micro program controlled Unit
	3 <sup>rd</sup>	Doubt clearing class
	4 <sup>th</sup>	<b>4.Memory System</b>
6 <sup>th</sup>	1 <sup>st</sup>	Memory characteristics
	2 <sup>nd</sup>	Memory hierarchy
	3 <sup>rd</sup>	RAM and ROM organization
	4 <sup>th</sup>	Interleaved Memory
	1 <sup>st</sup>	Cache memory

7th	2 <sup>nd</sup>	Virtual memory
	3 <sup>rd</sup>	Doubt clearing class
	4 <sup>th</sup>	<b>5.Input – Output System</b>
8th	1 <sup>st</sup>	Input Output Interface
	2 <sup>nd</sup>	Modes of Data Transfer
	3 <sup>rd</sup>	Programmed I/O Transfer
	4 <sup>th</sup>	Interrupt driven I/O
9th	1 <sup>st</sup>	DMA
	2 <sup>nd</sup>	I/O Processor
	3 <sup>rd</sup>	Revision
	4 <sup>th</sup>	<b>6.I/O Interface &amp; Bus architecture</b>
10th	1 <sup>st</sup>	Bus and System Bus
	2 <sup>nd</sup>	Types of System Bus
	3 <sup>rd</sup>	Data,Address,Control
	4 <sup>th</sup>	Bus Structure
11th	1 <sup>st</sup>	Basic Parameters of Bus design
	2 <sup>nd</sup>	SCSI,USB
	3 <sup>rd</sup>	<b>7.Parallel Processing</b>
	4 <sup>th</sup>	Linear Pipeline
12th	1 <sup>st</sup>	Multiprocessor
	2 <sup>nd</sup>	Flynn"s Classification
	3 <sup>rd</sup>	Revision
	4 <sup>th</sup>	Previous year question Disscution

Jayashree Bisshoi

SIGNATURE OF LECTURER

Biswaranjan Swain

SIGNATURE OF H.O.D