PNS SCHOOL OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL ENGINEERING

Branch: Electrical Engg.	Semester: 5TH	Name of the Lecturer: **Adity Narayan Jena**
Subject: DEM	Classes Alloted in a Week: 4	Duration of Semester: 14.07.2025 - 15.11.2025
Week	Class Day	Theory / Practical Topic
1st	1	**1.BASIC OF DIGITAL ELECTRONOICS** INTRODUCTION TO DIGITAL ELECTRONICS
	2	NUMBER SYSTEM(BINARY,OCTAL,DECIMAL,HEXADECIMAL)
	3	CONVERSION OF BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM INTO DECIMAL NUMBER SYSTEM
	4	CONVERSION OF DECIMAL NUMBER SYSTEM INTO BINARY/OCTAL/HEXADECIMAL NUMBER SYSTEM
2nd	1	CONVERSION OF BINARY TO OCTAL AND OCTAL TO BINARY,BINARY TO HEXADECIMAL AND HEXA-DECIMAL TO BINARY NUMBER SYSTEM,CONVERSION OF OCTAL INTO HEXADECIMAL AND HEXA-DECIMAL INTO OCTAL NUMBER SYSTEM
	2	BINARY ARITHMATIC (ADDITION,SUBTRACTION,MULTIPLICATION,DIVISION)
	3	1'S COMPLEMENT AND 2'S COMPLEMENT METHOD,SUBTRACTION USING 2'S COMPLEMENT
	4	BINARY CODES(BCD CODE,XS-3 CODE,GRAY CODE)
3rd	1	LOGIC GATES(AND,OR,NOT,NAND,NOR,XOR,XNOR) AND TRUTH TABLE
	2	UNIVERSAL GATE AND IMPLEMENTATION USING NAND AND NOR GATES
	3	DEMORGANS THEOREM AND ITS PROOF
	4	BOOLEAN ALGEBRA,SIMPLIFICATION OF LOGIC EXPRESSION USING BOOLEAN ALGEBRA
4th	1	BOOLEAN EXPRESSION(SOP,POS)
	2	2-VARIABLE,3-VARIABLE,4-VARIABLE K-MAP
	3	SIMPLIFICATION OF SOP AND POS EXPRESSION USING K-MAP
	4	DON'T CARE CONDITION
5th	1	**2.COMBINATIONAL LOGIC CIRCUIT** CONCEPT OF COMBINATIONAL LOGIC CIRCUIT, HALF ADDER CIRCUIT, WORKING
	2	HALF ADDER USING NAND GATES ONLY AND NOR GATES ONLY,FULL ADDER WORKING, LOGIC DIAGRAM
	3	REALIZE FULL ADDER USING TWO HALF-ADDERS AND AN OR-GATE WITH TRUTH TABLE,HALF SUBTRACTOR WORKING AND ITS LOGIC DIGRAM
	4	FULL SUBSTRACTOR WORKING,LOGIC DIAGRAM
6th	1	REVISION
	2	2:4 DECODER,3:8 DECODER WORKING,LOGIC DIAGRAM
	3	4:2 ENCODER,OCTAL TO BINARY ENCODER WORKING,BINARY-DECIMAL ENCODER WORKING,LOGIC DIAGRAM
	4	MUX,4:1 MUX WORKING,LOGIC DIAGRAM
7th	1	**3.SEQUENTIAL LOGIC CIRCUIT** DMUX,1:4 DMUX WORKING,LOGIC DIAGRAM
	2	1-BIT COMPARATOR AND 2-BIT COMPARATOR WORKING,TRUTH TABLE,LOGIC DIAGRAM
	3	SLC,TYPES OF SLC, DIFFERENCE BETWEEN CLC AND SLC,CONCEPT OF CLOCK AND TRIGGERING
	4	FLIP-FLOPS,NOR BASED SR-FF TRUTH TABLE AND WORKING
8th	1	NAND BASED SR-FF WORKING,CLOCKED NAND BASED SR-FF WORKING
	2	WORKING OF CLOCKED D-FF AND JK-FF
8th	3	RACE-AROUND CONDITION,WORKING OF MASTER-SLAVE JK-FF
	4	WORKING OF T FLIP-FLOP,APPLICATIONS OF FLIP-FLOPS
9th	1	COUNTERS, TYPES OF COUNTERS,DIFFERENCE BETWEEN ASYNCHRONOUS AND SYNCHRON-OUS COUNTER,MODULUS OF A COUNTER
	2	4-BIT ASYNCHRONOUS COUNTER,TIMING DIAGRAM

9th	3	REGISTERS AND ITS TYPES,WORKING OF SISO REGISTER
	4	WORKING OF SIPO AND PISO REGISTER
10th	1	WORKING OF PIPO REGISTER
	2	INTRODUCTION TO MICROPROCESSOR AND MICROCOMPUTER
	3	PIN DIAGRAM AND DESCRIPTION OF 8085 MICROPROCESSOR
	4	PIN DESCRIPTION OF 8085 MICROPROCESSOR
11th	1	REVISION
	2	BLOCK DIAGRAM/ARCHITECTURE OF 8085 MICROPROCESSOR
	3	ARCHITECTURE OF 8085
	4	REGISTERS OF 8085,STACK,STACK POINTER,STACK TOP
12th	1	**4.8085 MICROPROCESSOR** OPCODES, OPERANDS, INSTRUCTION TYPES ACCORDING TO BYTE SIZE (1-BYTE,2- BYTE,3-BYTE INSTRUCTIONS WITH EXAMPLES
	2	INSTRUCTION SET TYPES ACCORDING TO OPERATION PERFORMED BY MICROPROCESSOR (DATA TRANSFER, ARITHMATIC,LOGICAL,BRANCH,STACK,MACHINE CONTROL,I/O CONTROL)
	3	ADDRESSING MODES OF 8085 MICROPROCESSOR
	4	INSTRUCTION CYCLE, FETCH CYCLE,EXECUTION CYCLE,MACHINE CYCLE AND T-STATE
13th	1	TIMING DIAGRAM OF OPCODE FETCH CYCLE, MEMORY READ AND MEMORY WRITE CYCLE
	2	TIMING DIAGRAM OF I/O READ,I/O WRITE,MOV, MVI INSTRUCTION
	3	COUNTER AND TIME DELAY
	4	SIMPLE ASSEMBLY LANGUAGE PROGRAMMING OF 8085 MICROPROCESSOR
14th	1	**5.INTERFACING & SUPPORT CHIPS** BASIC CONCEPT OF INTERFACING, MEMORY MAPPING AND I/O MAPPING
	2	8255PPI PIN DESCRIPTION
	3	8255PPI FUNCTIONAL BLOCK DIAGRAM
	4	MODES OF 8255
15th	1	APPLICATION USING 8255 PPI-SEVEN SEGMENT LED DISPLAY
	2	SQUARE WAVE GENERATOR
	3	TRAFFIC LIGHT CONTROLLER
	4	REVISION

Signature of the Lecturer

Signature of the H.O.D.

Signature of the Principal